

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Priority** Application Serial No. .... 10/264,615  
**Priority** Filing Date ..... October 3, 2002  
 Inventor ..... Luan C. Tran  
 Assignee ..... Micron Technology, Inc.  
**Priority** Group Art Unit ..... 2813  
**Priority** Examiner ..... Laura M. Schillinger  
 Attorney's Docket No. .... MI22-2331  
 Title: Semiconductor Processing Methods of Forming Integrated Circuitry

**INFORMATION DISCLOSURE STATEMENT**

References - - See attached Form PTO-1449

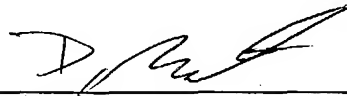
In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional of co-pending application Serial No. 10/264,615, filed October 3, 2002, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). Copies of the foreign references and publications are provided.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: July 11, 2003



Deepak Malhotra  
 Reg. No. 33,560  
 Wells, St. John, Roberts, Gregory & Matkin P.S.  
 601 W. First Avenue, Suite 1300  
 Spokane, WA 99201-3828  
 (509) 624-4276

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2152		SERIAL NO. Unknown	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
				FILING DATE Filed herewith		GROUP Filed herewith	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,612,629	09/16/86	HARARI	365	185	
	AB	4,785,342	11/15/88	YAMANAKA ET AL.	357	51	
	AC	5,786,249	07/28/98	DENNISON	438	241	
	AD	6,074,924	06/13/00	DENNISON ET AL.	438	306	
	AE	5,272,367	12/21/93	DENNISON ET AL.	257	306	
	AF	6,004,854	12/21/99	DENNISON ET AL.	438	306	
	AG	5,683,927	11/04/97	DENNISON ET AL.	437	57	
	AH	6,124,616	09/26/00	DENNISON ET AL.	257	369	
	AI	5,747,855	05/05/98	DENNISON ET AL.	257	369	
	AJ	5,534,449	07/09/96	DENNISON ET AL.	437	34	
	AK	5,706,806	07/07/98	DENNISON ET AL.	438	199	
	AL	5,773,863	06/60/98	BURR ET AL.	257	344	
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AM	EP 0 717 448 A1	06/19/96	EPO			
	AN	WO 98/29897	07/09/98	PCT			
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ		Silicon Processing for the VLSI Era, Vol. III; "Punchthrough (Subsurface-DIBL) in Short-Channel MOSFETs"; undated; pp. 232-235, 238-244				
	AR						
	AS						
EXAMINER				DATE CONSIDERED			
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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,661,054	8/26/1997	KAUFFMAN ET AL.	438	257	
	AB	5,736,444	4/07/1998	KAUFFMAN ET AL.	438	257	
	AC	6,337,250 B2	1/08/2002	FURUHATA	438	301	
	AD	6,312,997 B1	11/6/2001	TRAN	438	303	
	AE	6,455,362 B1	9/24/2002	TRAN ET AL.	438	194	
	AF						
	AG						
	AH						
	AI						
	AJ						
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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR						
	AS						
	AT						
EXAMINER				DATE CONSIDERED			
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